SILICON LOW NOISE AMPLIFIER CHIPS FOR MULTI-CHIP MODULE INTEGRATION ON A SILICON-BASED SUBSTRATE

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ABSTRACT

A method of designing low noise amplifier(LNA) using multi-chip module(MCM) technology is described here. First, low noise amplifier blocks using silicon BiCMOS process were fabricated. Noise figure and gain of 2-6 GHz were measured at different bias voltages after chips were fabricated. These chips were designed for multi-chip module integration on a newly developed low cost, low loss silicon substrate on which high-Q matching inductors are fabricated. Since the electrical characteristics of passive components on MCM are well controlled and the electrical characteristics of active devices are measured after fabrication, design accuracy and high yield can be achieved. Two design examples of low noise amplifiers at 2 GHz and 5 GHz are discussed. The 2 GHz LNA design utilizes high-Q spiral inductors as matching components whereas the 5 GHz LNA design utilizes microstrip lines as matching inductors.

INTRODUCTION

Building RFIC chips for wireless communication above 1 GHz by today's silicon technology has been of great interest because of its low cost advantage [1]. However, conductive substrate is still a major factor limiting silicon RFIC performance. For example, the input matching network of a low noise amplifier (LNA) usually requires a high Q inductor which is not easy to realize on conductive silicon substrate. Also, the cross talk of synthesizer and LNA integrated on a same silicon substrate limits the sensitivity of radio receivers.

Multi-chip module (MCM) integration on high resistivity silicon substrate provides a good solution for this. This type of chip level packaging allows passive components requiring high quality factor to be fabricated on a low cost and low loss substrate [2]. It also absorbs the parasitics associated with conventional packaging into chip level packaging and thus can be better modeled and controlled. RFIC chips are then flip-chip mounted on the MCM substrate with those critical matching networks on it. Figure 1 shows the cross sectional view of MCM integration.

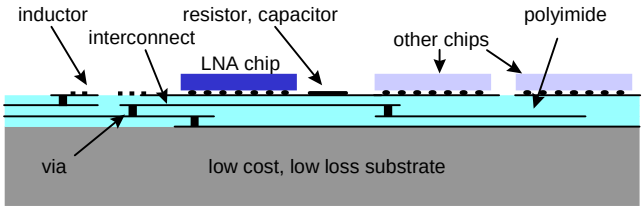

Fig. 1 Multi-chip module integration of RF circuits.

In this paper, we present a design of LNA using BiCMOS technology and flip-chip MCM package. The multi-stage amplifier consists of identical gain blocks whose gain and noise figure can be tuned by varying the supply voltage. By setting up the appropriate bias voltage at each stage, the amplifier's performance can be optimized. The noise parameters of gain block at various bias

0-7803-4603-6/97/$5.00 (c) IEEE

conditions were measured and two LNAs at 2 GHz and 5 GHz were designed.

AMPLIFIER CHIP

The LNA block designed in common-emitter configuration was fabricated on silicon BiCMOS process. The main transistor used in the circuit is a six-emitter-finger (Ae = 6x0.6x12.8 μm^2 = 46.08 μm^2) bipolar transistor with f_{max} about 8 GHz at Ic = 4 mA. A small bipolar transistor with Ae = 0.36 μm^2 is used as current mirror to control the bias current. This is the smallest available device on this process and was chosen to minimize the effect on noise figure. A 15 kΩ resistor was selected to have a bias current of 5 mA around 3 V supply. The single-bias design allows easy integration with less complexity in bias network. Layout and schematics of the LNA block are shown in Figures 2 and 3, respectively. The chip layout is designed for both on-wafer test and flip-chip mount so that chips can be tested before packaging. The size of the chip is 0.8 x 1.1 mm^2.

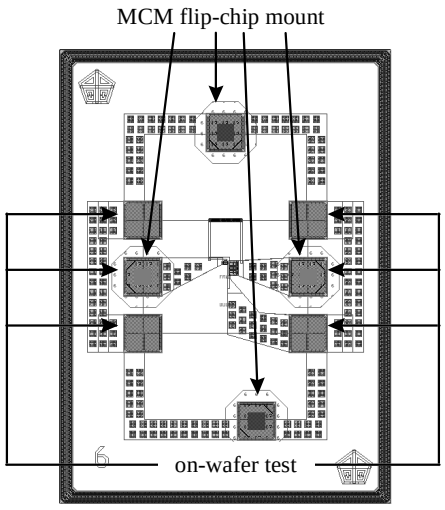

Fig. 2 Chip layout of silicon gain block

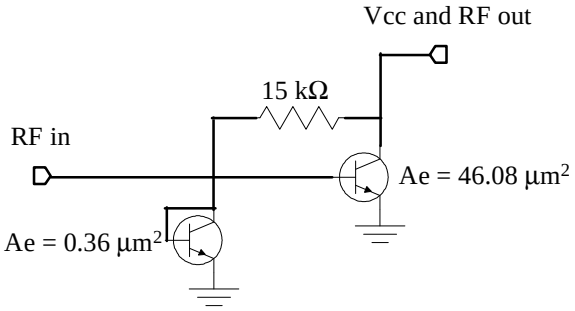

Fig. 3 Schematics of gain block.

NOISE CHARACTERIZATION

The LNA chip was characterized on a source-pull noise measurement system. Minimum noise figure(NFmin), optimal matching impedance(Γopt), noise resistance(Rn), and associated gain(Gas) at different bias voltages were measured. Figure 4 shows measured NFmin and Gas of 2-6 GHz at different bias voltages and currents. These data along with measured S-parameters were stored in a CAD file for various LNA designs at different frequencies for different applications. For example, the PCS LNA design could use the data at 2 GHz and the WLAN LNA design could use the data at 2.5 or 5 GHz [3]. The noise data shows different behaviors at 2 GHz and 5 GHz. At 2 GHz, the minimum noise figure increases as the voltage and current increase. At 5 GHz, however, the minimum noise figure hits the lowest value at 2-2.5 V. This results in different choices of bias voltage in LNA design.

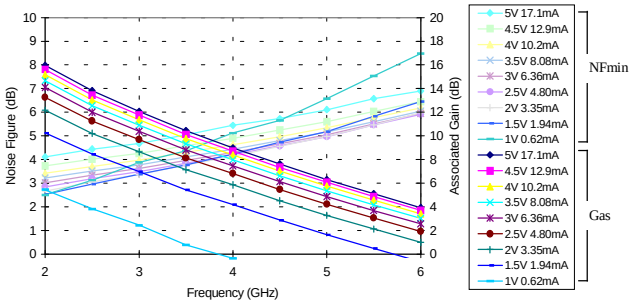

Fig. 4 Measured minimum noise figure and associated gain.

LNA DESIGN

Two amplifiers were designed based on the measured data of gain block. One is at 2 GHz and the other is at 5 GHz. Since low noise is desired and the total gain needs to be greater than 15 dB, multiple stage LNA design was used. The cascaded noise figure follows the equation:

$$NF_{total} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \cdots$$

For the amplifier at 2 GHz, a bias voltage of 1.5 V was chosen for the first stage since it provides the lowest NFmin at 2.5 dB and an adequate gain around 10 dB. A bias voltage of 2 V would increase the gain to around 12 dB but will also increase the noise figure and current consumption. It is not necessary since second stage will provide enough gain to reach 15 dB target. When designing the second stage, gain is the first factor to consider. Since the target is 15 dB, same bias voltage of 1.5 V providing gain around 10 dB will easily cover the gap. Therefore, a two-stage LNA with each stage biased at 1.5 V was designed. Figure 5 shows its schematics. The cascaded noise figure and gain are 3.3 dB and 16.9 dB, respectively. VSWR at input or output is better than 2.5:1. Low pass filter with R-C bypass is integrated with DC bias line to ensure low frequency stability. Total current consumption is less than 4 mA.

For the amplifier at 5 GHz, the lowest minimum noise figure occurs around 2-2.5 V. However, the gain of 4 dB at 2.5 V is too low that the noise from the following stages would affect the total noise figure. By increasing the bias voltage to 3.5 V, the minimum noise figure does not change much but the gain increases to over 5 dB. Continuing the increase of bias voltage would increase the noise faster than gain, and also increase the current consumption. Therefore, the first stage biased at 3.5 V was determined. Since the gain at first stage is low, the noise figure at the following stage becomes as important as its gain. It is also observed that the available gain at 5 GHz is too low that a three-stage design has to be used to achieve 15 dB gain. It is also desired to keep the power consumption low. Considering the above factors, a three-stage amplifier with each stage biased at 3.5 V were designed. The schematics is similar to the one in Figure 5 except that an additional stage is added. The cascaded noise figure and gain are 6.5 dB and 15.0 dB, respectively. VSWR at input or output is better than 2:1. The total current consumption is less than 25 mA with a 3.5 V supply.

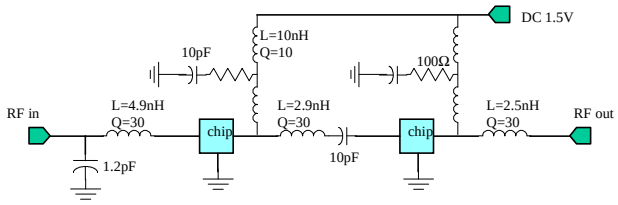

Fig. 5 Low noise amplifier at 2 GHz

Matching networks in these amplifier circuits all use high Q inductors. These inductors will be fabricated on a newly developed low cost, low electrical loss, and high thermal conductivity silicon substrate. Inductors with Q greater than 30 have been demonstrated on 2kΩ-cm high-resistivity silicon substrate[4]. With even smaller loss tangent, the inductor Q on this new substrate is expected to be higher. At 2 GHz, rectangular spiral inductors are used. These inductors can be designed very accurately with measured substrate characteristics implemented into a good inductor model[5]. At 5 GHz, high-Q inductor with small inductance does not have many turns and naturally becomes microstrip line structure when inductance is small enough. In addition, a straight microstrip line is free from the current crowding effect which appears in the spiral inductor due to strong magnetic field at center[5][6].

The fabrication of integrated inductor requires two layers of metal. They are separated by polyimide and the connection is made by via process. Aluminum with 3μm of thickness is used in each metal layer. The thickness of polyimide in each layer is 5μm. In addition to inductors, resistors and capacitors can also be fabricated. The layout of MCM integration of 2 GHz LNA is shown in Figure 6.

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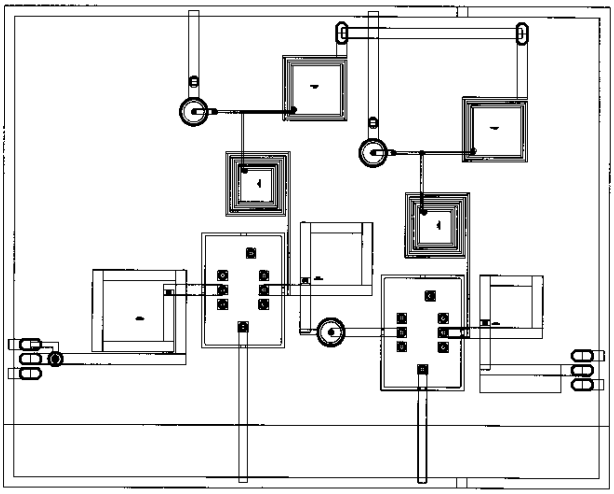

Fig. 6 Multi-Chip Module integration of 2 GHz LNA

CONCLUSION

A low noise amplifier block using silicon BiCMOS process was developed for multi-chip module integration. By varying the bias voltage of the chip and designing matching networks on MCM substrate, Low noise amplifiers at different frequency for different applications were designed by using the same chip. This method of using identical gain blocks to build amplifiers for different applications is suitable for low cost, high volume production. Since the matching network is designed based on the measured data after chips are fabricated, the performance of circuit will have less variation than traditional MMIC design. It should be noted that devices of other technologies, e.g., Bipolar or GaAs MESFET, may be used for the chip design to achieve better performance.

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